IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

FUTURE LINK SYSTEMS, LLC,	§	
	§	
Plaintiff,	§	C.A. No. 6:21-cv-363-ADA
v.	§	
	§	JURY TRIAL DEMANDED
REALTEK SEMICONDUCTOR CORP.,	§	
	§	
Defendant.	§	

DEFENDANT REALTEK SEMICONDUCTOR CORP.'S
MOTION FOR SANCTIONS UNDER FED. R. CIV. P. 11

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I. INTRODUCTION

Plaintiff Future Link Systems, LLC ("FLS") never should have filed this case. Had it done ***any*** reasonable pre-suit investigation, it would have known before filing its complaint that its infringement claims against Realtek Semiconductor Corp. ("Realtek") were baseless. Realtek identified these deficiencies to FLS after it filed, but FLS has pressed ahead anyway, necessitating the present motion.

To begin, FLS has yet to offer a single fact that would support its direct infringement claims. Despite a complete lack of any evidence that Realtek makes, sells, or imports accused products in the United States, FLS not only maintained its claims, but renewed them in its amended complaint even after Realtek identified this lack of evidence correspondence and in its motion to dismiss.

In addition, FLS has based its infringement claims on a handful of technical documents published by third-party Arm Ltd. ("ARM"). Those documents do not describe Realtek products. Moreover, the technical documents that FLS cites (1) expressly state that the quality-of-service ("QoS') product features that FLS accuses of meeting necessary claim elements are ***optional,*** and (2) demonstrate that the QoS signals are ***not used*** in the ARM processors at issue. Not a shred of evidence suggests that the required features are present in any Realtek accused products. Even a minimally adequate pre-suit investigation would quickly have concluded that these documents provide no basis to assert that Realtek's products meet all the limitations of any of the asserted claims. But FLS apparently did not even read the documents it cited, and it now maintains its claims despite Realtek having identified these deficiencies.

Worse yet, FLS avoided—for months—responding to Realtek's concerns about its unfounded allegations and its inadequate investigation, or even communicating with Realtek's counsel about these and other deficiencies. Even now, FLS has refused to address these deficiencies in discussions with Realtek. As a result, FLS has forced Realtek to engage in motions practice to address its persistence in litigating meritless claims.

FLS's ongoing abuse of the legal process requires sanctions. FLS's claims are based on nothing but speculation, and its lawsuit is a fishing expedition in a lake without fish. Because FLS's

own evidence shows its claims to be unfounded, this Court should dismiss this case with prejudice and award Realtek its reasonable attorney fees and other expenses incurred in defending against this frivolous suit.

II. FLS HAS PERSISTED IN ASSERTING ITS CLAIMS AGAINST REALTEK DESPITE BEING SHOWN THAT THE CLAIMS HAVE NO FACTUAL BASIS

A. FLS Asserts Unfounded Infringement Claims in its Original Complaint.

On April 13, 2021, FLS filed its original complaint alleging that Realtek products that "use processors supporting ARM AMBA AXI4 or newer, including without limitation the RTD1295" ("Originally Accused Chips") infringe U.S. Patent No. 7,917,680 (the "'680 Patent"). ECF No. 1 ("Complaint") ¶ 14. But FLS's allegations lacked *any* factual support for multiple aspects of its claims.

As an initial matter, FLS alleged that Realtek "makes, uses, offers for sale, sells, and/or imports" the Originally Accused Chips in, or into, the United States. *Id.* But FLS acknowledged that Realtek is "organized under the laws of Taiwan, with its principal place of business at No. 2 Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan." Complaint ¶ 2. Yet it offered no basis for its free-floating belief that Realtek conducts business within the United States or performs any other act classified under 35 U.S.C. § 271(a), nor any other facts in support of its conclusory allegations of direct infringement. *See generally* Complaint.

The Complaint also offered no basis to believe that any Realtek product actually includes the technology that FLS accuses of infringement. FLS relied almost exclusively on reference manuals and protocol specifications published by ARM. Indeed, the only technical information specific to a Realtek product that FLS included anywhere in its Complaint or the attached infringement chart was that the RTD1295 contains an ARM Cortex-A53 processor. *See* ECF No. 1-2 at 2 ("OC Chart"). Otherwise, FLS's infringement allegations chiefly cited the ARM Cortex-A53 Technical Reference Manual, Issue J (June 13, 2018) ("TRM"), *see, e.g.*, OC Chart at 3, and the ARM AMBA AXI and ACE Protocol Specification, Issue D (Oct. 28, 2011) ("AXI Spec"),[1] *see, e.g.*, *id.* at 4-5, throughout its supposed

[1] A copy of the TRM is attached hereto as Ex. 8, and a copy of the AXI Spec is attached hereto as Ex. 9.

comparison of the RTD1295's features to the claims of the '680 Patent. In particular, FLS asserted that the Cortex-A53 includes an AMBA AXI4 ("AXI4") bus, *see* OC Chart at 5, and that the limitation in claim 1 reciting "generating a performance-based communications order for passing the packet data" reads only on quality-of-service ("QoS") features described in the AXI Spec. *See id.* at 11-12.

However, FLS did not reveal (indeed, it did not appear to even notice) that QoS is an *optional* feature of the AXI4 bus protocol that it relied upon. *See* AXI Spec §§ 8.1.1, A.10.3. FLS further neglected to mention that the ARM TRM it cited lists each and every signal on both versions of the Cortex-A53's memory interface, and that no QoS signals appear on either list. *See* TRM §§ A.10-A.11.[2] In short, FLS offered no reason to believe that an RTD1295, or any other Realtek product, includes the optional QoS feature, and its own documents directly *contradict* its assertion that Cortex-A53 products include the QoS features that FLS accuses of infringement. Taken together, these startling oversights cast grave doubt on the adequacy of FLS's pre-suit investigation.

B. FLS Refuses to Engage in Discussions Prior to Realtek Filing its Original Motion to Dismiss.

Prior to its deadline to answer the Original Complaint, counsel for Realtek reached out to FLS's counsel, seeking to discuss the basis for FLS's apparently baseless infringement allegations. ECF No. 13-3 ¶¶ 4-6. Although FLS's counsel promised to respond with additional information the following day, not a single attorney representing FLS did so. *Id.* ¶ 8. Rather than engage in good-faith discussions, FLS's counsel instead refused to answer any further communications. *Id.* ¶¶ 9-11; ECF No. 13-4.

With no other recourse, Realtek filed its original motion to dismiss, which among other things described FLS's lack of any factual basis to allege (a) that Realtek makes, sells, or imports its products in the United States, (b) that any Realtek products use the accused technology, and (c) that FLS

[2] Nor did FLS address the fact that the Cortex-A53 can be configured with one of two different memory interfaces, neither of which is an AXI4 bus. *See* OC Chart at 3; TRM § 1.2.2 (noting the memory interface can be an ACE or a CHI bus, but not mentioning AXI4). As discussed herein, however, the Court need not reach this issue, as the evidence cited by FLS shows that ***none*** of an AXI4 bus, an ACE bus, or a CHI bus have the accused QoS features.

properly served Realtek with the complaint and summons. ECF No. 13. FLS never responded to Realtek's motion, nor has it ever detailed its pre-suit investigation or articulated any good-faith basis for its infringement allegations.

C. FLS Asserts Expanded but Equally Unfounded Infringement Claims in its First Amended Complaint.

Instead of responding to Realtek's motion to dismiss—or even meeting to confer about the basis for its infringement claims—FLS filed its First Amended Complaint ("FAC") on July 15, 2021, a week after its deadline to respond to Realtek's well-founded motion to dismiss had expired. ECF No. 18. The FAC remains the live complaint in this action. However, the FAC was as frivolous as the original Complaint, for many of the same reasons (and a few new ones), and thus demonstrated that FLS put no more investigation behind its amended complaint than the original.

As a threshold matter, the FAC asserted frivolous and legally unsupported arguments that Realtek had waived the jurisdictional and service arguments made in its motion to dismiss. FAC ¶ 11. FLS cited no authority for its position. *Id.* Nor did FLS acknowledge, much less grapple with, the long-standing black letter law contrary to its frivolous waiver argument. *Id.*; *see* also ECF No. 20 at 19-20 (citing governing precedent). FLS never bothered to defend its unfounded assertion of waiver in any subsequent filing.

Despite being on notice that Realtek does not operate in the United States, FLS again alleged direct infringement. *E.g.*, FAC ¶¶ 5, 19, 21. However, the FAC, like the original Complaint, offered no factual basis for its allegations that Realtek imports, makes, uses, sells, or offers to sell any accused product within the United States. *See generally* FAC. Instead, FLS relied exclusively on third-party offers, made through Amazon, to sell non-Realtek products that allegedly contain Realtek chips, without alleging any factual basis for connecting those sales with Realtek. *See* FAC ¶¶ 7-9.

The FAC also expanded its list of accused products to include "products that use processors supporting ARM AMBA AXI4 or newer *and/or ARM AMBA CHI*, including without limitation the Realtek RTD1295, RTD1296, RTD1395, RTD1315, RTD1319, and RTD1619" ("Accused Chips")

(emphasis added).[3] Yet it purported to rely on the same deficient OC Chart attached to its original complaint. FAC ¶ 22. As discussed above, the infringement allegations in that chart were based on ***optional*** features of the Cortex-A53 processor not shown to be present on the RTD1295 or any other Realtek product identified by FLS. *Supra* 3. In addition, the OC Chart contains no allegations concerning the CHI standard whatsoever (which was referenced for the first time in the FAC), nor did the FAC allege that Realtek products actually use a CHI bus, much less set forth a factual basis for any such belief. *See generally* OC Chart. Separately, the FAC purported to rely on the Preliminary Infringement Contentions FLS served on Realtek on July 8, 2021. FAC ¶ 22. But FLS did not file its contentions or in any other way put those contentions before this Court or make them part of the record in this case. And in any case, the nonpublic Preliminary Infringement Contentions and Preliminary Infringement Chart[4] also failed to cite or discuss the portions of the AXI Spec showing that QoS features are optional or the portions of the TRM showing that no QoS signals are present on the interfaces FLS accuses of infringement. *See generally* Exs. 1-2 and *infra* at 9-17.

In short, the documents cited by FLS once again failed to provide any plausible factual support for FLS's assertions of infringement. To date, FLS has yet to articulate any reason to believe that the technology it accuses of infringement actually exists in any Realtek product, nor has it even asserted that any such belief was formed after a reasonable investigation, pre-filing or otherwise.[5]

D. Realtek Notifies FLS That its Claims Are Groundless, But FLS Refuses to Withdraw its Allegations.

On Sept. 16, 2021, Realtek served its Preliminary Invalidity Contentions on FLS. Ex. 3. In its contentions, Realtek specifically laid out multiple deficiencies in FLS's Preliminary Infringement

[3] FLS has charted only the RTD1295, but asserts that all Accused Chips "operate in substantially the same way for purposes of infringement." Ex 2 at 1 ("Preliminary Infringement Chart").

[4] Because FLS has yet to make these documents part of the record, Realtek has attached FLS's Preliminary Infringement Contentions as Ex. 1 and its Preliminary Infringement Chart as Ex. 2.

[5] Because the FAC provided no meaningful response to the grounds for dismissal that Realtek raised in its original motion, Realtek filed its Renewed Motion to Dismiss for Lack of Personal Jurisdiction and Lack of Standing. ECF No. 20 ("Renewed Motion"). The grounds for that Motion to Dismiss are entirely independent of the bases for the present motion.

Contentions, including many of those noted above. *Id.* at 2-5. FLS offered no response.

On Sept. 22, 2021, Realtek followed up with further correspondence to FLS's counsel, specifically putting FLS and its counsel on notice under *Stone Basket Innovations, LLC v. Cook Med. LLC*, 892 F.3d 1175, 1180-81 (Fed. Cir. 2018) that FLS's FAC and infringement contentions are objectively baseless in multiple ways that a reasonable pre-suit investigation would readily have revealed. Ex. 4 ("*Stone Basket* Letter"). The *Stone Basket* Letter also identified the portions of the TRM and AXI Spec, on which FLS itself based its FAC and contentions, that demonstrate that the QoS features accused of infringing required claim limitations simply do not exist in the products FLS accused. *Id.* at 3-10. It also included an express notice that Realtek would seek Rule 11 sanctions if FLS refused either to explain how it could maintain infringement allegations against Realtek or to withdraw its suit by Oct. 1, 2021. *Id.* at 11-12; *see also Stone Basket*, 892 F.3d at 1181. FLS did not withdraw or explain its claims, or indeed respond in any way. Ex. 5.

Realtek reached out to FLS one final time on Oct. 4, 2021, reiterating Realtek's willingness to meet and confer to avoid further motions practice. Ex. 5. Finally, and for the first time, FLS responded, but only to insist its allegations were adequate and to decline to confer any further. Ex. 6. FLS again failed to offer any substantiation for its core contention that QoS features are found in any accused Realtek product.

Accordingly, on Oct. 26, 2021 Realtek served this Motion on FLS and noted that it would file the Motion 21 days later unless FLS withdrew its baseless claims. *See* Ex. 7; Fed. R. Civ. P. 11(c)(2).

III. THIS COURT SHOULD DISMISS FLS'S BASELESS CLAIMS AND AWARD REALTEK ITS ATTORNEY FEES AS SANCTIONS UNDER RULE 11.

A. Legal Standard

Rule 11 of the Federal Rules of Civil Procedure imposes a basic threshold of good faith that "is aimed at curbing abuses of the judicial system." *Bus. Guides, Inc. v. Chromatic Commc'ns Enters., Inc.*, 498 U.S. 533, 542 (1991). Under Rule 11, "[a] signature certifies to the court that the signer has read the document, has conducted a reasonable inquiry into the facts and the law and is satisfied that the document is well grounded in both, and is acting without any improper motive." *Id.* Moreover,

"a litigant's obligations with respect to the contents of these papers are not measured solely as of the time they are filed with or submitted to the court, but include reaffirming to the court and advocating positions contained in those pleadings and motions after learning that they cease to have any merit." Fed. R. Civ. P. 11 Advisory Committee Notes to the 1993 Amendments.

Patent cases are no exception. At a bare minimum, "the evidence uncovered by the patent holder's investigation must be sufficient to permit a reasonable inference that all the accused products infringe." *Antonious v. Spalding & Evenflo Cos.*, 275 F.3d 1066, 1075 (Fed. Cir. 2002). Therefore, "in bringing a claim of infringement, the patent holder, if challenged, must be prepared to demonstrate to both the court and the alleged infringer exactly why it believed ***before filing the claim*** that it had a reasonable chance of proving infringement. Failure to do so should ordinarily result in the district court expressing its broad discretion in favor of Rule 11 sanctions." *View Eng'g, Inc. v. Robotic Vision Sys., Inc.*, 208 F.3d 981, 986 (Fed. Cir. 2000) (emphasis added).

In patent cases, Rule 11 motions are decided under regional circuit law. *See ResQNet.com, Inc. v. Lansa, Inc.*, 594 F.3d 860, 873 (Fed. Cir. 2010). In the Fifth Circuit, courts determine whether there was a Rule 11 violation under "an objective, not subjective standard of reasonableness under the circumstances." *Raylon, LLC v. Complus Data Innovations, Inc.*, 700 F.3d 1361, 1367 (Fed. Cir. 2012). "Thus, an attorney violates Rule 11(b)(3) when an objectively reasonable attorney would not believe, based on some actual evidence uncovered during the prefiling investigation, that each claim limitation reads on the accused device." *Antonious*, 275 F.3d at 1074.

Once a violation has been established, "the court may impose an appropriate sanction on any attorney, law firm, or party that violated the rule or is responsible for the violation." Fed. R. Civ. P. 11(c)(1). Rule 11 sanctions may include an award of "reasonable attorney's fees and other expenses directly resulting from the violation." Fed. R. Civ. P. 11(c)(4). District courts may also "dismiss baseless claims or defenses as sanctions" under Rule 11. *Mr. Mudbug, Inc. v. Bloomin' Brands, Inc.*, 770 Fed. Appx. 658, 661 (5th Cir. 2019) (quoting *Thomas v. Capital Sec. Servs., Inc.*, 836 F.2d 866, 878 (5th Cir. 1988) (en banc)); *see also Vehicle Operation Techs. LLC v. Am. Honda Motor Co.*, 67 F.Supp.3d 637, 652-53 (D. Del. 2014) ("as here the entire suit is objectively baseless, any lesser

sanction [than dismissal] would be ineffective").

B. FLS Filed Frivolous Infringement Claims Based on a Grossly Inadequate Pre-Suit Investigation.

1. FLS has never identified any facts in support of its direct infringement allegations.

Direct infringement cannot exist unless the accused party makes, uses, sells, or offers to sell the patented invention *within the United States*, or imports the patented invention *into the United States*. 35 U.S.C. § 271(a). "It is the general rule under United States patent law that no infringement occurs when a patented product is made and sold in another country." *Microsoft Corp. v. AT&T Corp.*, 550 U.S. 437, 441 (2007). "As the Supreme Court has stated, if one desires to prevent the selling of its patented invention in foreign countries, its proper remedy lies in obtaining and enforcing foreign patents." *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 831 F.3d 1369, 1379 (Fed. Cir. 2016) (citing D*eepsouth Packing Co. v. Laitram Corp*, 406 U.S. 518, 531 (1972)).

FLS's original Complaint alleges that Realtek "has transacted business in this District and has committed acts of direct infringement … in this District by, among other things, importing, offering to sell, and selling products that infringe the asserted patents." Complaint ¶ 6; *see also id.* ¶¶ 5, 14, 18 (alleging direct infringement by "making, using, offering for sale, selling and/or importing into the United States" the accused products). But as any reasonable pre-suit investigation would have revealed, Realtek makes and sells its products in Asia, not the United States. *See, e.g.*, ECF No. 20-2 ¶ 8. FLS has never identified a single act performed by Realtek that could constitute direct infringement under § 271(a). *See generally* FAC.

Thus, it is no surprise that FLS failed to plead a single fact that supports its direct infringement allegations. *See generally* Complaint. It appears that FLS never gathered any relevant facts to support a direct infringement claim, despite its clear obligation to perform an adequate pre-suit investigation. When challenged by Realtek, *see* ECF No. 13 at 3, 9-10, FLS did not defend its direct infringement allegations. It merely filed its FAC and added allegations regarding sales by third parties on Amazon, without alleging a single fact connecting those sales with Realtek. *See* FAC ¶¶ 5, 7-9, 10, 19, 23. The fact that FLS added these allegations without alleging a single fact regarding ***Realtek's*** conduct in the

United States demonstrates that it re-pled its direct infringement claims *knowing* that they had no factual basis as to Realtek. When challenged in Realtek's Renewed Motion to Dismiss, *see* ECF No. 20 at 2-3, 8, FLS again failed even to address its direct infringement allegations, much less defend them, *see generally* ECF No. 23. Its most recent response is equally silent. Ex. 6.

In short, FLS has never identified any evidence of even a single act of direct infringement by Realtek, it has not articulated any reason to believe that one has occurred, and it has not described any pre-filing investigation that would support the assertion of its direct infringement claims. By failing to investigate the required facts, asserting baseless direct infringement claims, and then maintaining them when Realtek repeatedly challenged the basis for the claims, FLS and its counsel violated Rule 11 over and over again.

2. Every instance of FLS's infringement allegations attacking the AXI4 standard are refuted by its own cited documents.

The inadequacy of FLS's pre-suit investigation is further illustrated by the fact that it has directed infringement allegations to a QoS feature of the AXI4 bus protocol that cannot possibly exist on Realtek's Accused Chips. Nor is any proprietary information needed to reach this obvious conclusion—the technical documents that FLS itself cited clearly demonstrate that the QoS features that form the basis of its infringement claims cannot be present.

Each of the independent claims of the '680 Patent includes claim limitations that recite ordering and/or communicating packet data based on performance-based rules.[6] To meet each of these limitations, FLS purports to identify a quality-of-service ("QoS") feature of the AXI4 bus protocol specification. Specifically, FLS's charts cite documents that indicate that the RTD1295 includes an

[6] *See* ECF No. 1-1 Claim 1 (reciting "generating a performance-based communications order for passing the packet data as a function of performance-based rules" and "communicating the packet data as a function of the performance-based communications order"); Claim 8 (reciting "a performance arbiter configured and arranged to order the packet data for communication on the communications link as a function of the communications priority" and "a controller configured and arranged for controlling the passage of the packet data on the communications link as a function of the packet data ordering"); Claim 20 (reciting "a performance arbiter circuit configured to reassign an order to the packets based upon the … performance-based rules" and "a communications circuit to communicate the packets in the reassigned order").

ARM Cortex-A53 processor, and that the ARM Cortex-A53 memory interface can be configured either as an ACE bus or as a CHI bus,[7] but not as an AXI4 bus.[8] *E.g.*, Ex. 2 at 2, 3-4, 7-8, 15 (citing the ARM Cortex-A53 Technical Reference Manual, Issue J (June 13, 2018) ("TRM")); OC Chart at 3.[9] Nevertheless, FLS purports to identify QoS features described in the specifications for the AXI4 protocol, as meeting the limitations noted above. *See, e.g.*, Ex. 2 at 21-23 ("the RTD1295 orders packet data communications based on the AXI4 or later QoS systems" (citing ARM's AMBA AXI and ACE Protocol Specification, Issue D (Oct. 28, 2011) ("AXI Spec") §§ 8.1, 8.3)), 25-26 ("the Accused Products may further order packet data communications based on the CHI QoS system" (citing ARM's AMBA 5 CHI Architecture Specification, Issue E.a (Aug. 19, 2020) ("CHI Spec") §§ 10.1-10.2)), 65, 73, 110-111, 113-114.

Even as to the AXI4 bus, however, the documents on which FLS itself purports to rely for these allegations show that QoS signals and features *are not present* in any AXI4 interface of the ARM Cortex-A53 processor.

To begin, the AXI Spec specifically notes that QoS signals are "[o]ptional."

Table A10-1 Master interface write channel signals and default signal values

Signal	Description	Direction	Required?	Default

…

[7] FLS's infringement allegations concerning CHI are addressed in the following section. *Infra* 16-17.

[8] FLS has cited no facts supporting the notion that any Realtek product supports AXI4. Instead, its OC Chart—the only claim-by-claim comparison that FLS has ever put on the record in this case—cited only a portion of the TRM identifying a memory interface that can be configured to support the AMBA 4 ACE (not AXI4) protocol or the AMBA 5 CHI protocol. OC Chart at 3. Specifically, as the TRM cited by FLS shows, the Cortex-A53 memory interface cannot be configured as an AXI4 interface—instead it is either an ACE or CHI interface. TRM § 1.2.2. But FLS does not purport to chart features of the ACE bus protocol. *See generally* OC Chart. And it offered no facts suggesting that either version of this interface can support any version of the AXI protocol, or that any Realtek product is configured to do so. *Id.* Nevertheless, the Court need not reach this issue, since the evidence cited by FLS (as discussed above) does not show that the accused QoS signals exist in ***any*** of an AXI4 bus, an ACE bus, or a CHI bus.

[9] For brevity, the remainder of this section cites only the Preliminary Infringement Chart attached as Ex. 2. However, the OC Chart is equally, if not more, flawed.

AWQOS	QoS value	Output	Optional	0b0000

AXI Spec §§ A10.3 Table A10-1 (annotation added);

Table A10-3 Master interface read channel signals and default signals values

Signal name	Description	Direction	Required?	Default
		...		
ARQOS	QoS value	Output	Optional	0b0000

id. A10.3 Table 10-3 (ARQOS) (annotation added); *see also*

A8.1.1 QoS interface signals

The AXI4 signal set is extended to support two 4-bit QoS identifiers:

AWQOS A 4-bit QoS identifier, sent on the write address channel for each write transaction.

ARQOS A 4-bit QoS identifier, sent on the read address channel for each read transaction.

In this specification, **AxQOS** indicates **AWQOS** or **ARQOS**.

The protocol does not specify the exact use of the QoS identifier. This specification recommends that **AxQOS** is used as a priority indicator for the associated write or read transaction. A higher value indicates a higher priority transaction.

A default value of 0b0000 indicates that the interface is not participating in any QoS scheme.

Note

Additional interpretations of the QoS identifier can be used.

id. § 8.1.1 ("A default value of 0b0000 [on a QoS signal] indicates that the interface *is not participating in any QoS scheme*." (emphasis added)). FLS has never provided a basis for a good-faith belief that QoS signals are present in any AXI4 interface that may exist on a Cortex-A53 processor (including its memory interface), or that any Realtek Accused Chip implements the optional AXI4 QoS scheme.

Second, to the extent that FLS might belatedly assert that the ACE protocol implements AXI4 (without ever having made such an allegation in its pleadings or contentions), the TRM on which FLS relied affirmatively shows that QoS signals and features are absent from the ACE version of the memory interface of the Cortex-A53 processor that FLS accuses. Specifically, the TRM provides lists of signals for the Cortex-A53's ACE memory interface. *See* TRM § A.11. But that list conspicuously omits the AXI4 QoS signals—ARQOS and AWQOS—identified by FLS. In other words, the TRM cited by FLS shows that FLS's infringement allegations against AXI4 are wholly baseless.

For example, the AXI Spec expressly names the optional QoS signal governing write transactions (AWQOS) as a write address channel signal.

Table A2-2 Write address channel signals

Signal	Source	Description
AWID	Master	Write address ID. This signal is the identification tag for the write address group of signals. See *Transaction ID* on page A5-77.
AWADDR	Master	Write address. The write address gives the address of the first transfer in a write burst transaction. See *Address structure* on page A3-44.
AWLEN	Master	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This changes between AXI3 and AXI4. See *Burst length* on page A3-44.
AWSIZE	Master	Burst size. This signal indicates the size of each transfer in the burst. See *Burst size* on page A3-45.
AWBURST	Master	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated. See *Burst type* on page A3-45.
AWLOCK	Master	Lock type. Provides additional information about the atomic characteristics of the transfer. This changes between AXI3 and AXI4. See *Locked accesses* on page A7-95.
AWCACHE	Master	Memory type. This signal indicates how transactions are required to progress through a system. See *Memory types* on page A4-65.
AWPROT	Master	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. See *Access permissions* on page A4-71.
AWQOS	Master	*Quality of Service*, QoS. The QoS identifier sent for each write transaction. Implemented only in AXI4. See *QoS signaling* on page A8-98.
AWREGION	Master	Region identifier. Permits a single physical interface on a slave to be used for multiple logical interfaces. Implemented only in AXI4. See *Multiple region signaling* on page A8-99.
AWUSER	Master	User signal. Optional User-defined signal in the write address channel. Supported only in AXI4. See *User-defined signaling* on page A8-100.
AWVALID	Master	Write address valid. This signal indicates that the channel is signaling valid write address and control information. See *Channel handshake signals* on page A3-38.
AWREADY	Slave	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. See *Channel handshake signals* on page A3-38.

AXI Spec §§ A2.2 Table A2-2. But while the TRM's list of write address channel signals for the ACE memory interface includes many other write address channel signals identified in the AXI spec, it does not include the optional signal AWQOS.

A.11.2 Write address channel signals

Table A-19 shows the write address channel signals for the ACE interface.

Table A-19 Write address channel signals

Signal	Direction	Description
AWADDRM[43:0]	Output	Write address.
AWBARM[1:0]	Output	Write barrier type.
AWBURSTM[1:0]	Output	Write burst type.
AWCACHEM[3:0]	Output	Write cache type.
AWDOMAINM[1:0]	Output	Write shareability domain type.
AWIDM[4:0]	Output	Write address ID.
AWLENM[7:0]	Output	Write burst length.
AWLOCKM	Output	Write lock type.
AWPROTM[2:0]	Output	Write protection type.
AWREADYM	Input	Write address ready.
AWSIZEM[2:0]	Output	Write burst size.
AWSNOOPM[2:0]	Output	Write snoop request type.
AWUNIQUEM	Output	For WriteBack, WriteClean and WriteEvict transactions. Indicates that the write is: 0 Shared. 1 Unique.
AWVALIDM	Output	Write address valid.

TRM § A.11.2 Table A-19.

Similarly, the AXI Spec expressly names the optional QoS signal governing read transactions (ARQOS) as a read address channel signal.

Table A2-5 Read address channel signals

Signal	Source	Description
ARID	Master	Read address ID. This signal is the identification tag for the read address group of signals. See *Transaction ID* on page A5-77.
ARADDR	Master	Read address. The read address gives the address of the first transfer in a read burst transaction. See *Address structure* on page A3-44.
ARLEN	Master	Burst length. This signal indicates the exact number of transfers in a burst. This changes between AXI3 and AXI4. See *Burst length* on page A3-44.
ARSIZE	Master	Burst size. This signal indicates the size of each transfer in the burst. See *Burst size* on page A3-45.
ARBURST	Master	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated. See *Burst type* on page A3-45.
ARLOCK	Master	Lock type. This signal provides additional information about the atomic characteristics of the transfer. This changes between AXI3 and AXI4. See *Locked accesses* on page A7-95.

ARCACHE	Master	Memory type. This signal indicates how transactions are required to progress through a system. See *Memory types* on page A4-65.
ARPROT	Master	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access. See *Access permissions* on page A4-71.
ARQOS	Master	*Quality of Service*, QoS. QoS identifier sent for each read transaction. Implemented only in AXI4. See *QoS signaling* on page A8-98.
ARREGION	Master	Region identifier. Permits a single physical interface on a slave to be used for multiple logical interfaces. Implemented only in AXI4. See *Multiple region signaling* on page A8-99.
ARUSER	Master	User signal. Optional User-defined signal in the read address channel. Supported only in AXI4. See *User-defined signaling* on page A8-100.
ARVALID	Master	Read address valid. This signal indicates that the channel is signaling valid read address and control information. See *Channel handshake signals* on page A3-38.
ARREADY	Slave	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. See *Channel handshake signals* on page A3-38.

AXI Spec § A2.5 Table A2-5. Again, the TRM's list of read address channel signals for the ACE memory interface includes most of the signals specifically identified in the AXI Spec, but not ARQOS.

A.11.5 Read address channel signals

Table A-22 shows the read address channel signals for the ACE master interface.

Table A-22 Read address channel signals

Signal	Direction	Description
ARADDRM[43:0]	Output	Read address. The top 4 bits communicate only the ACE virtual address for DVM messages. The top 4 bits are Read-as-Zero if a DVM message is not being broadcast.
ARBARM[1:0]	Output	Read barrier type.
ARBURSTM[1:0]	Output	Read burst type.
ARCACHEM[3:0]	Output	Read cache type.
ARDOMAINM[1:0]	Output	Read shareability domain type.
ARIDM[5:0]	Output	Read address ID.
ARLENM[7:0]	Output	Read burst length.
ARLOCKM	Output	Read lock type.
ARPROTM[2:0]	Output	Read protection type.
ARREADYM	Input	Read address ready.
ARSIZEM[2:0]	Output	Read burst size.
ARSNOOPM[3:0]	Output	Read snoop request type.
ARVALIDM	Output	Read address valid.

TRM § A.11.5 Table A-22.

As a result, any reasonable pre-suit investigation would have concluded that the ACE version of the Cortex-A53's memory interface *does not include any QoS signals*. FLS apparently did not conduct that reasonable investigation. Despite the fact that the technical documents that FLS referenced showed its allegations to be entirely baseless, FLS nevertheless filed this action in reliance on nonexistent QoS features. Moreover, even though Realtek has now identified this obvious and fatal flaw in FLS's investigation, FLS has made no effort whatsoever to defend its allegations against AXI4 and refuses to withdraw its infringement claims against products with AXI4 or ACE versions of the Cortex-A53's memory interface. *See* Ex. 6 (addressing CHI alone).

FLS has never identified any AXI4 or ACE interface in the RTD1295 or any other Realtek product as infringing other than the memory interfaces discussed above, *supra* 9-10, and thus FLS cannot justify its decision to bring this suit on such a basis. Moreover, to the extent that FLS mentioned other alleged AXI4 or ACE interfaces in passing, its allegations are equally frivolous. First, while the TRM reveals that the Cortex A-53 processor *may* contain an Accelerator Coherency Port ("ACP") that is implemented as an AXI4 interface, the TRM also shows that (a) the ACP is entirely optional, and (b) even when it is present, the ACP does not include QoS signaling.

7.7 ACP

The optional *Accelerator Coherency Port* (ACP) is implemented as an AXI4 slave interface with the following restrictions:

- 128-bit read and write interfaces.
- **ARCACHE** and **AWCACHE** are restricted to Normal, Write-Back, Read-Write-Allocate, Read-Allocate, Write-Allocate, and No-Allocate memory. **ARCACHE** and **AWCACHE** are limited to the values `0b0111`, `0b1011`, and `0b1111`. Other values cause a SLVERR response on **RRESP** or **BRESP**.
- Exclusive accesses are not supported.
- Barriers are not supported. The **BRESP** handshake for a write transaction indicates global observability for that write.
- **ARSIZE** and **AWSIZE** signals are not present and assume a value of `0b100`, 16 bytes.
- **ARBURST** and **AWBURST** signals are not present and assume a value of INCR.
- **ARLOCK** and **AWLOCK** signals are not present.
- **ARQOS** and **AWQOS** signals are not present.
- **ARLEN** and **AWLEN** are limited to values 0 and 3.

TRM § 7.7. Second, although FLS appears also to rely on a technical reference manual for the ARM

CoreLink NIC-400 Network Interconnect, *see* Ex. 2 at 25, 29, 42, 69, 76, 116, FLS cites no evidence that the RTD1295 includes a CoreLink NIC-400 Network Interconnect, much less one that is configured to include optional QoS features. *See* ARM CoreLink NIC-400 Network Interconnect Technical Reference Manual[10] §§ 1.2 (QoS features "are separately licensed and are not included in the NIC-400 base product"), 2.4 (QoS listed as an "additional service[] that [is an] extension[] to the CoreLink NIC-400 Network Interconnect"), A.3.1 (AWQOS signal exists "[o]nly when [QoS is] enabled by the GUI"), A.3.4 (ARQOS signal exists "[o]nly when [QoS is] enabled by the GUI; *Id.* Table 3-1 (QoS registers are "only present when the QoS settings … have been set to programmable").

Therefore, the documents FLS has cited show that the AXI4 QoS features it accuses cannot and do not exist on the Cortex-A53 processor. Nor has FLS satisfied its burden to show any other good-faith reason to believe that QoS features exist in any Realtek product. Finally, FLS has never identified any other feature of the RTD1295, or any other Realtek product, that meets the claim limitations noted above, for which FLS relies exclusively on the cited QoS signals. In short, FLS's infringement claims are baseless and frivolous, as its pre-suit investigation should have revealed.

3. FLS's new infringement allegations attacking CHI are equally unsupported.

As noted above, FLS has never filed anything in this case stating even a single factual allegation concerning the CHI interface that was referenced in passing in its FAC, despite purporting to accuse products that ***may*** implement CHI in its FAC. *Supra* 4-5. The only document FLS has ever provided to document its investigation of the CHI protocol is its unfiled Preliminary Infringement Chart. There, as it did with AXI4, FLS asserts that required elements of each of its asserted claims are met exclusively by QoS features of the CHI protocol. *See, e.g.*, Ex. 2 at 25-26 ("the Accused Products may further order packet data communications based on the CHI QoS system" (citing ARM's AMBA 5 CHI Architecture Specification, Issue E.a (Aug. 19, 2020) ("CHI Spec") §§ 10.1-10.2)), 30, 69-70, 76, 85, 112-113, 118, 127.[11]

[10] A copy of this specification is attached hereto as Ex. 10.

[11] A copy of the CHI Spec is attached hereto as Ex. 11.

FLS's allegations are flawed in at least two ways. First, FLS bears the burden to show a good-faith reason to believe that a feature it accuses is present in the accused products. But FLS has never shown any reason to believe that ***any*** Realtek product implements CHI. Second, FLS's slipshod investigation of CHI, like its investigation of AXI4, apparently did not extend even to the rest of the documents that it cites. The ARM TRM cited by FLS also provides a list of signals for the CHI version of the Cortex-A53's memory interface. *See* TRM § A.10. As with the ACE interface, no QoS signals appear anywhere on that list. *See* TRM §§ A.10-A.10.8. Nor has FLS, when it finally responded to Realtek's repeated communications, identified any QoS signals in the Cortex-A53. Ex. 6. And finally, FLS has never pointed to any other possible CHI interface, in any Realtek product.

In short, FLS has not even plausibly shown that its investigation provided a good-faith reason to believe that any CHI interface exists in a Realtek product or that that QoS signals it accuses of infringement would be present in any CHI interface, if one actually did exist. As a result, FLS's allegations concerning the CHI protocol are wholly unsupported and cannot meet the standards required by Rule 11.

C. Dismissal and Award of Realtek's Attorney Fees and Other Expenses Are the Appropriate Sanctions for FLS's Filing and Maintenance of Frivolous Claims.

Where a plaintiff bases its patent infringement claims on an identified product feature, without having a reasonable basis for alleging that the feature exists in the accused products, the entire suit is "objectively baseless" and dismissal is appropriate under Rule 11. *Vehicle Operation*, 67 F.Supp.3d at 653. This is especially true where a reasonable pre-suit investigation would have affirmatively revealed that the allegedly infringing feature does not even exist.

Judge Andrews's opinion in *Vehicle Operation* is instructive. There, the plaintiff had asserted against a plethora of automobile manufacturers a patent relating to presenting status information on a "display." *Id.* at 641-42. During prosecution, the inventor had both disclaimed the plain meaning of "display" and "specifically disclaimed any type of display other than a 'dedicated display' [that] present[ed] the relevant information 'at all times.'" *Id.* However, for each manufacturer, publicly-available documents—such as the accused car's user manual—or the plaintiff's own pleadings showed

that the display accused by the plaintiff showed different user-selectable information at different times and therefore was not "dedicated." *Id.* at 643-48. As a result, there was "no doubt … that if the Plaintiff's attorneys had performed the requisite pre-suit investigation, as, for example by looking at the relevant pages of the owner's manual, it would have been evident that the accused vehicles did not meet the display limitation" of the asserted patent. *Id.* at 651. Taken together, those documents made clear—to anyone who actually read the entirety of the documents—that any infringement claim accusing those displays was doomed, so the "entire suit [was] objectively baseless" and dismissal was the only appropriate sanction. *Id.* at 653 ("any lesser sanction would be ineffective").

The same is true here. FLS's infringement allegations are directed to a figment of FLS's own imagination: QoS features (which do not exist based on FLS's cited documents) that FLS nevertheless alleges are present in the Accused Chips. No reasonable investigation could possibly have concluded that its infringement claims could succeed. FLS accused a variety of Realtek chips of infringing claims that recite ordering and/or communicating packet data based on performance-based rules. *Supra* 2-3, 5. Every pleading and document filed or served by FLS has identified only QoS features of an AXI4 bus as meeting the recited limitation. But as in *Vehicle Operation*, two publicly available documents, taken together, show that the accused QoS features are not present in the accused products. First, the AXI Spec expressly states that the QoS features FLS accuses are merely *optional* parts of the standard. *Supra* 10-11. That alone should stop any plaintiff from bringing infringement claims based solely on the alleged existence of an AXI4 bus. But, again as in *Vehicle Operation*, a second publicly available document confirms what the first merely suggested: the TRM for the Cortex-A53 processor conclusively shows that the AXI4 QoS features FLS accused are *not* present in the Cortex-A53 processor that FLS identifies as the infringing component in Realtek's accused products. *Supra* 11-15.

These two documents were known to FLS. FLS relied upon both documents heavily in the infringement chart it submitted to this Court, and again in its infringement contentions. *Supra* 2-5. FLS and its counsel apparently failed to read "the relevant pages," *Vehicle Operation*, 67 F. Supp.3d at 651, or otherwise conduct even the minimal investigation required to show that the features it

accused of infringement actually exist. FLS's "entire suit is objectively baseless" as a result. *Id.* at 653.

FLS's woefully deficient pre-suit investigation therefore falls well below the level required of parties and officers of this Court under Rule 11 and easily justifies dismissal. Its conduct *since* filing the original Complaint removes all doubt that dismissal is the appropriate sanction.

As detailed above, Realtek has made multiple attempts to discuss the numerous and basic deficiencies outlined herein with FLS, to no avail. Prior to its answer deadline, Realtek reached out to FLS's counsel to discuss various deficiencies in FLS's original Complaint. *Supra* 3. Although FLS promised to respond, its counsel reneged on that promise and cut off communications for several days. *Supra* 3. With no other recourse, Realtek filed its original Motion to Dismiss, but FLS failed to file any response. *Supra* 3-4. Instead, more than a week after its response to Realtek's motion was due, FLS filed its FAC, in which it attempted to dismiss all of Realtek's arguments as waived (despite long-standing black letter law to the contrary), but offered no substantive response. The FAC also purported to expand the list of accused products. *Supra* 4. But FLS failed to include any new factual support for its existing deficient infringement allegations concerning the AXI4 standard, and offered literally nothing on the record in support of its new allegations concerning the CHI standard. *Supra* 5. Instead, FLS relied on the same flawed and incomplete infringement chart attached to its original Complaint. *Supra* 5. Separately, the FAC purported to rely on its Preliminary Infringement Contentions and Preliminary Infringement Chart, without actually filing them. *Supra* 5. But FLS's throwaway reference to an unfiled document in its FAC cannot possibly satisfy Rule 11 standards. And when it finally—after months of unanswered emails, responded to Realtek's repeated overtures—FLS said only that its allegations were adequate and insisted on Realtek providing evidence that its products do ***not*** contain a CHI bus or QoS features as a condition of further discussions, rather than demonstrating that its allegations are supported by any evidence. Ex. 6.

Finally, the manner in which FLS has litigated its flawed jurisdictional and service of process positions in this matter only underscores its clearly established pattern of resistance, delay, and refusal to communicate with Realtek's counsel. As noted above, FLS has steadfastly refused to meet and

confer with Realtek's counsel on either issue, both in advance of Realtek's first motion to dismiss and since. *Supra* 2-3. Moreover, when finally forced to offer some defense of its alleged service, FLS not only attempted—again—to rely on documents it has never filed with this Court, *see* ECF No. 23 at 11-14 (purporting to rely on two unfiled declarations regarding service of process), it also failed even to defend the legality of its chosen method of service under Taiwanese law, as required by the Federal Rules. ECF No. 24 at 7-9; ECF No. 28-1. To date, FLS has never sought to properly serve Realtek. Instead, it has forced Realtek to file and oppose multiple motions stretching over the course of four months.

FLS's obstinate refusal to withdraw its baseless accusations, and its dilatory and vexatious litigation of at least the service-of-process issue, have imposed significant and improper burdens on Realtek, measured in both time and treasure. They amply justify dismissal of this action. *See, e.g.*, *Vehicle Operations*, 67 F.Supp.3d at 651 ("[t]he Plaintiff's attorneys' continued insistence to litigate this matter, even after being apprised by the Defendants that the accused products could not possibly infringe, further highlights that the Plaintiff's attorneys simply turned a blind eye to the actual [products] that they were accusing of infringement.").

Furthermore, as Realtek has demonstrated, FLS has never articulated a factual basis for its claims in either the original Complaint or the FAC. *Supra* 8-17. Thus, FLS's case has been baseless since the day the original Complaint was filed, and all of Realtek's expenses—including attorney fees—incurred in defending this case "directly result[] from the violation" of Rule 11. Fed. R. Civ. P. 11(c)(4). As a result, this Court can and should award all of Realtek's expenses and fees in this action as an additional sanction under Rule 11. *See, e.g.*, *Merriman v. Sec. Ins. Co. of Hartford*, 100 F.3d 1187, 1194 (5th Cir. 1996) (awarding all fees incurred defending frivolous claims because "[a]ttorneys' fees are an appropriate sanction designed to deter frivolous litigation").

IV. CONCLUSION

For at least the reasons set forth above, Realtek respectfully requests that the Court grant this motion and dismiss FLS's claims against Realtek with prejudice as a sanction under Rule 11.

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Respectfully Submitted

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CERTIFICATE OF SERVICE

The undersigned certifies that on November 18, 2021, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3). Any other counsel of record will be served by a facsimile transmission or first-class mail.

/s/ Jeffrey L. Johnson
Jeffrey L. Johnson